

Customer Engineering Diagrams

**CONTROL DATA[®]
169 AUXILIARY
MEMORY UNIT**

RECORD of REVISIONS

[illegible]

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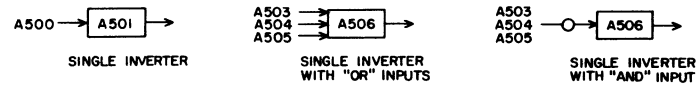
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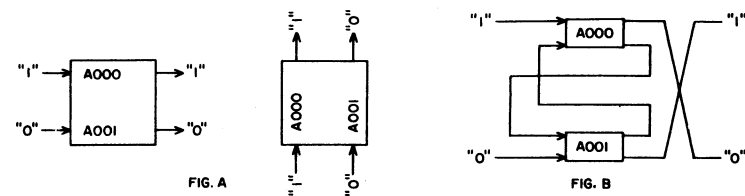
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SYMBOLS

SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.

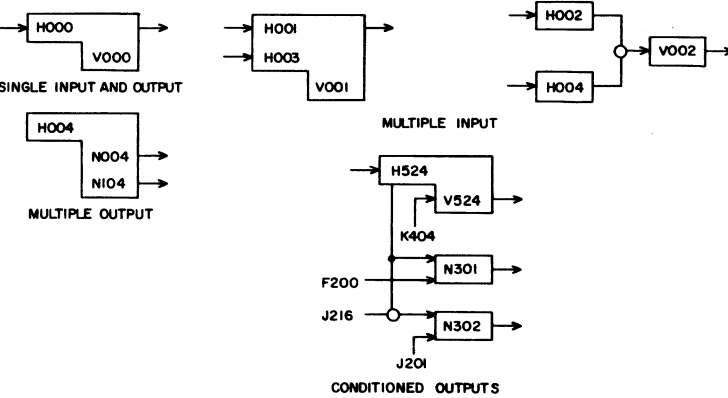


FLIP-FLOP (FF) - The flip-flop is a storage device with two stable states, designated "1" (or Set) and "0" (or Clear), and is composed of two inverters. The logical symbol (Fig. A) is a square that is formed by the combination of two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper or left half of the symbol and "0" (or Clear) inputs and outputs are shown with the lower or right half of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in Fig. B.

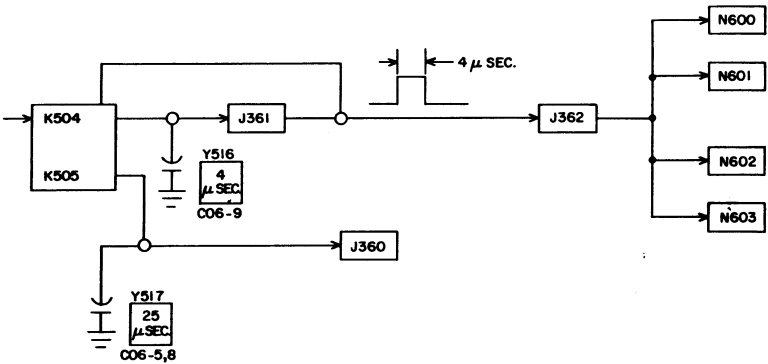


CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microseconds). Conventions which apply to control delays are:

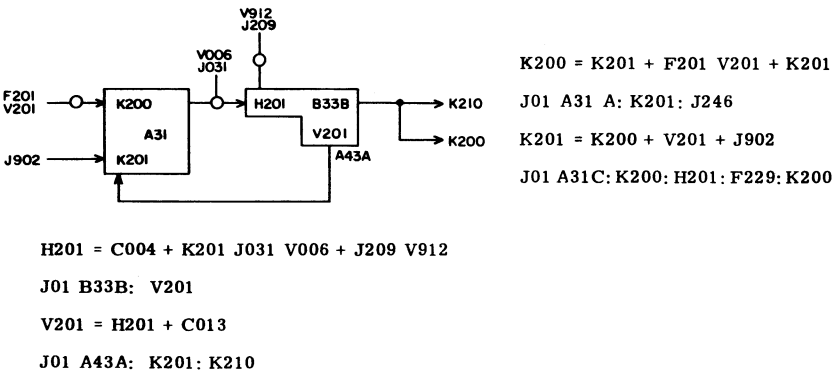
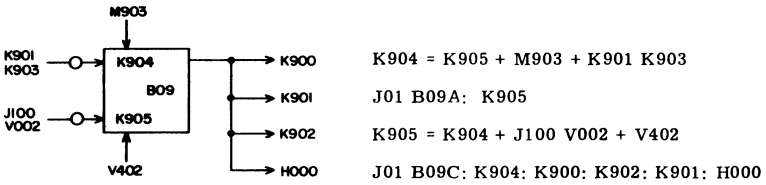
1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase, and an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.



CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made. The output waveform may be omitted.

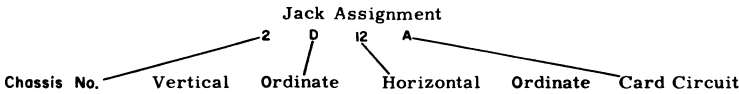


SYMBOL REPRESENTATION OF TYPICAL EQUATIONS



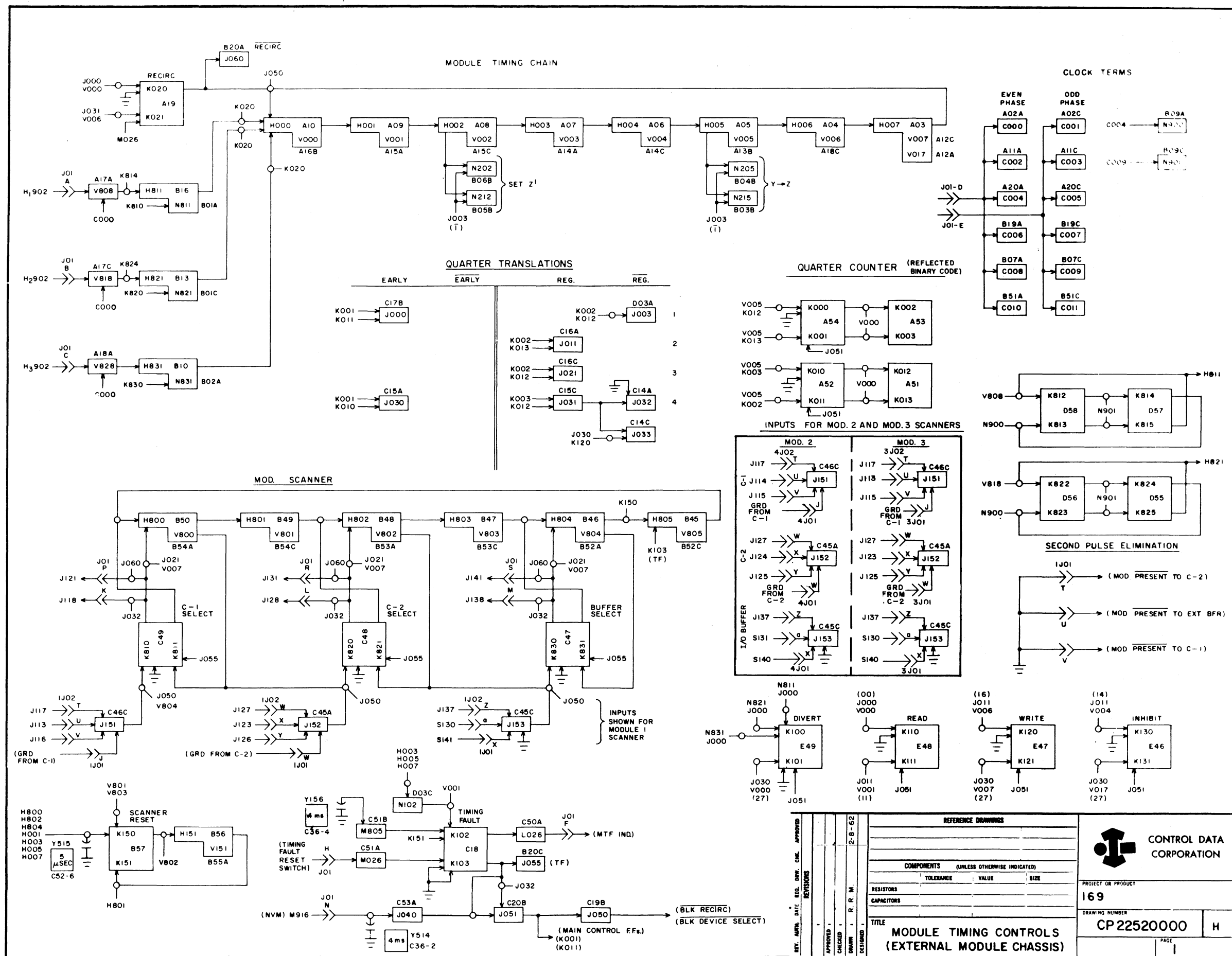
JACK ASSIGNMENTS

The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.

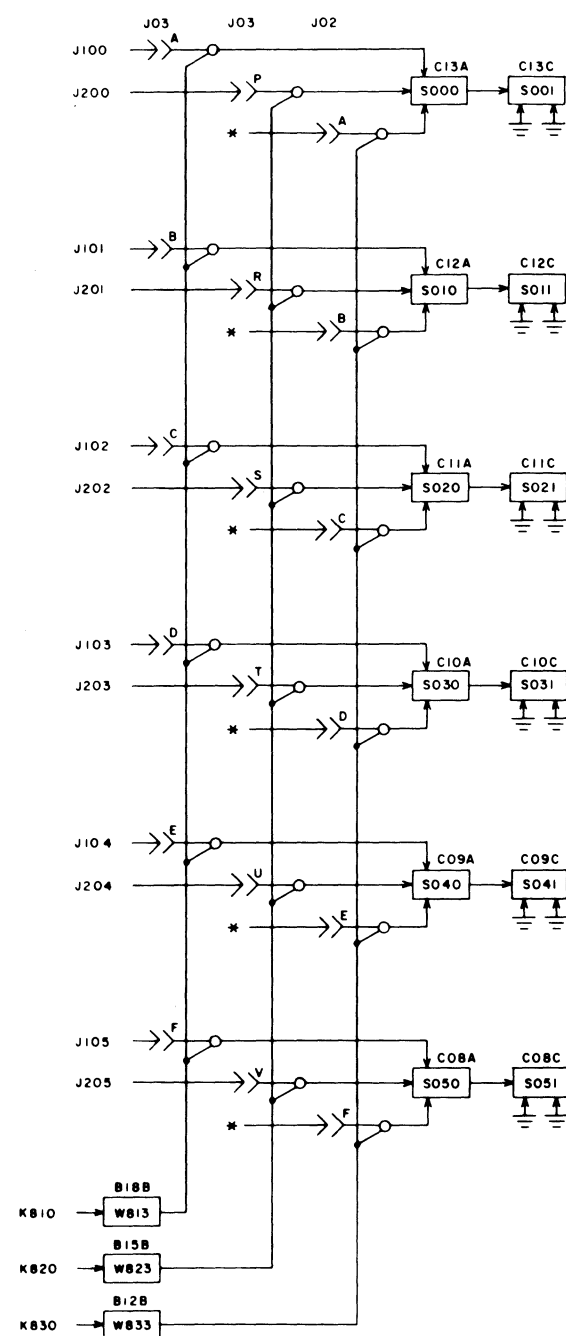


- Conventions which apply to jack assignments shown on the diagrams:
1. When most of the jack assignments on a diagram are on a common chassis, the chassis number is omitted from the jack assignments for this chassis and specified in a note on the diagram.
 2. The omission of the card circuit letter from a jack assignment indicates card circuit B. (For flip-flops which indicate one jack assignment for both inverters, the omission of the card circuit letter indicates card circuit A for the even-numbered inverter and card circuit C for the odd-numbered inverter.)

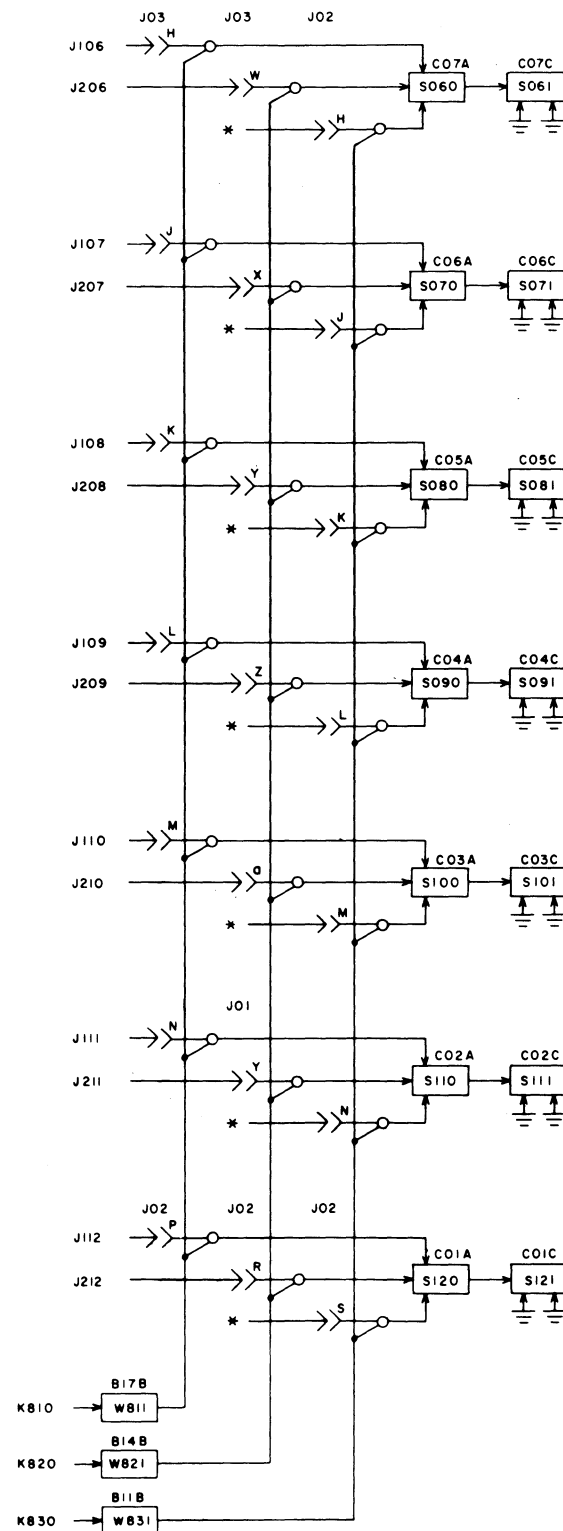
KEY TO SYMBOLS USED ON LOGIC DIAGRAMS



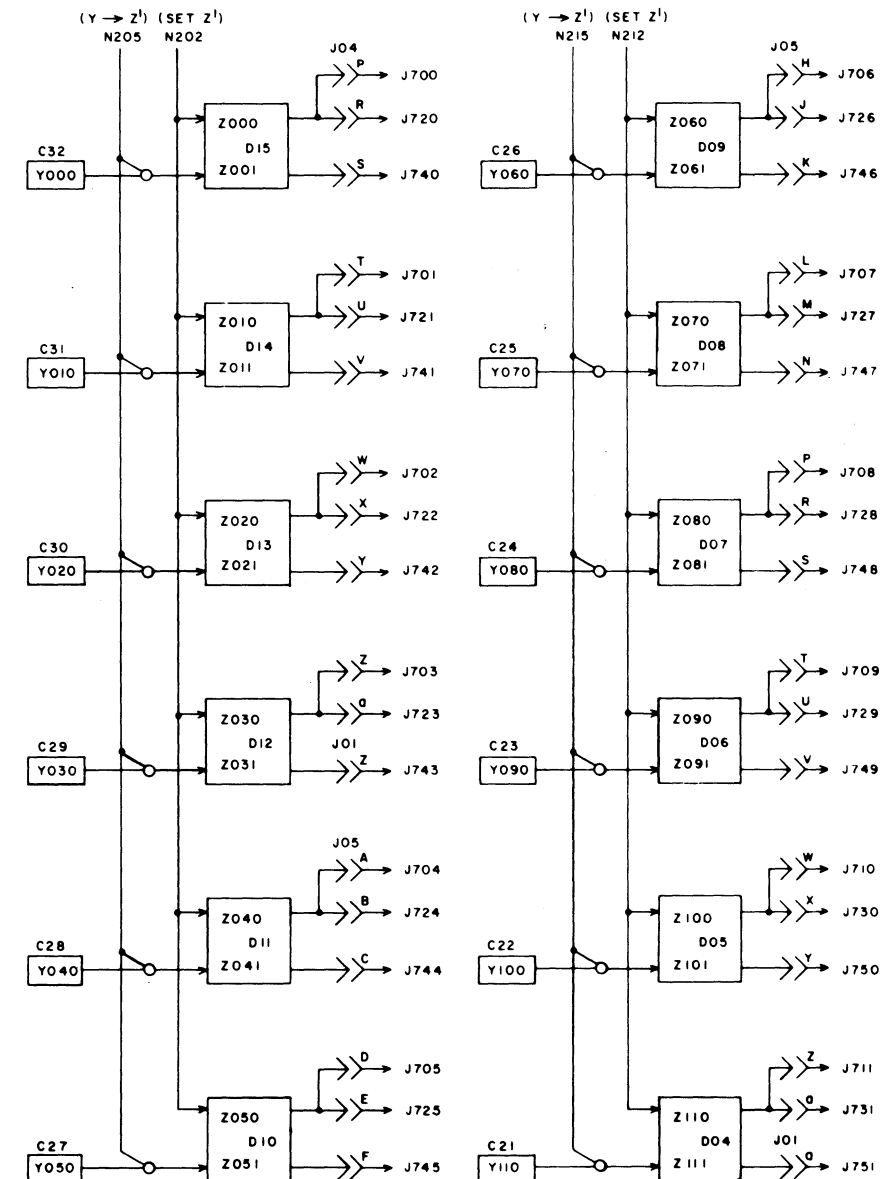
S' INVERTERS



* EXTERNAL BFR INPUTS TO S' INVERTERS ARE SHOWN UNDER (BER) → S' ON DWG XCP225204.

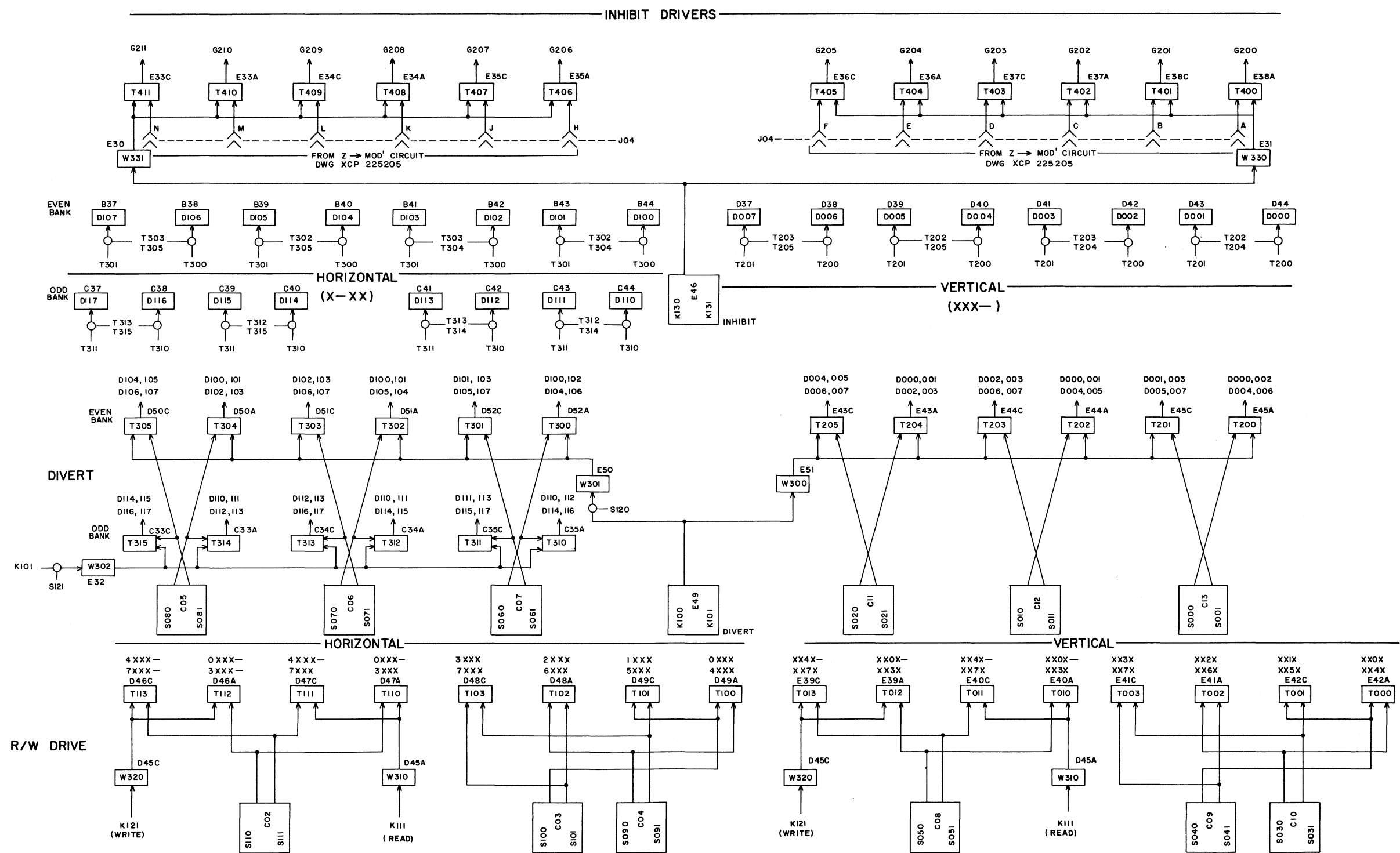


Z' REGISTER



Y000 - Y110 ARE MEMORY SENSE AMPLIFIERS (TYPE 57)

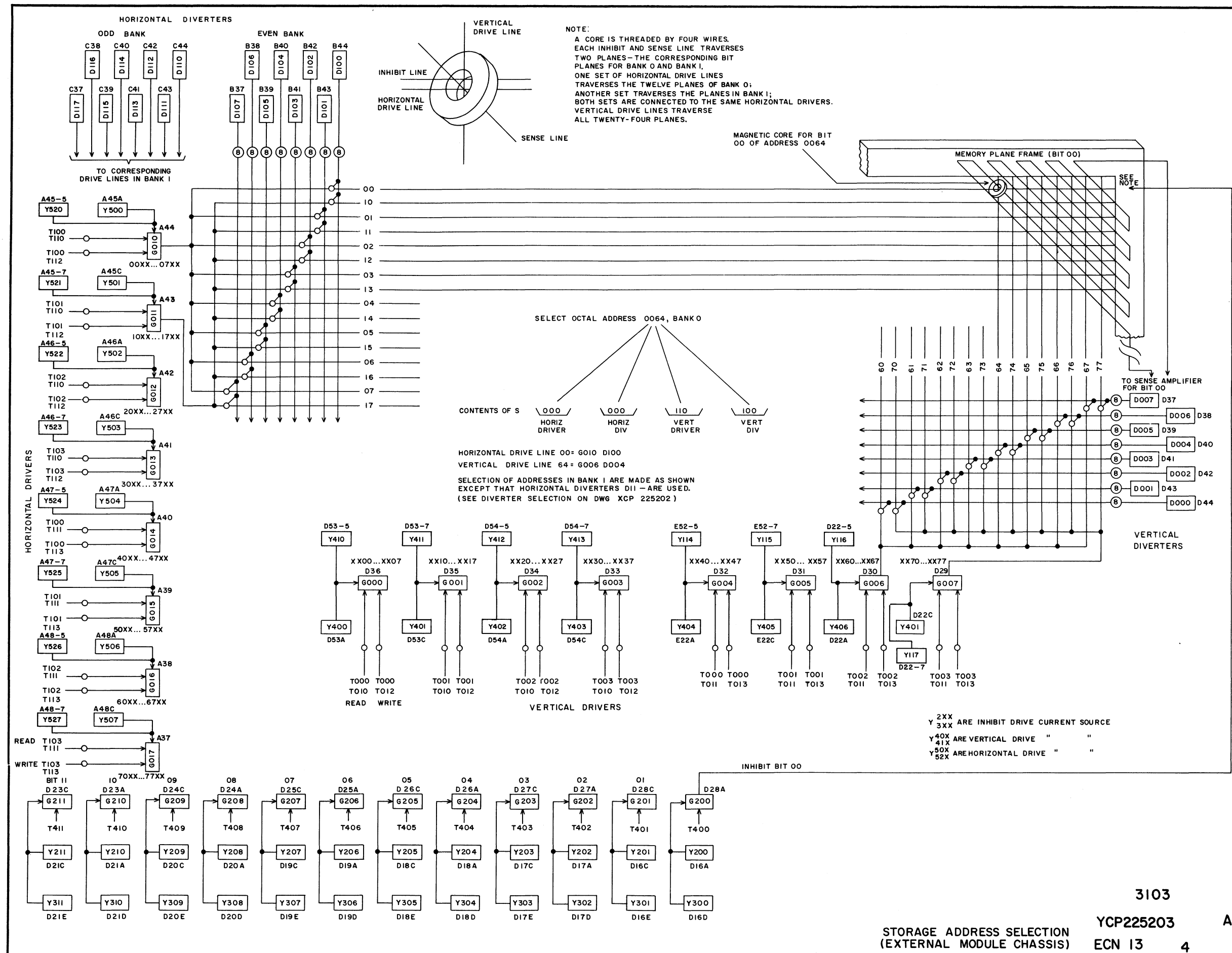
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	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	TOLERANCE	VALUE	
	RESISTORS	SIZE	
CAPACITORS		TITLE S' INVERTERS & Z' REGISTER (EXTERNAL MODULE CHASSIS)	
ECN 15		PAGE 2	

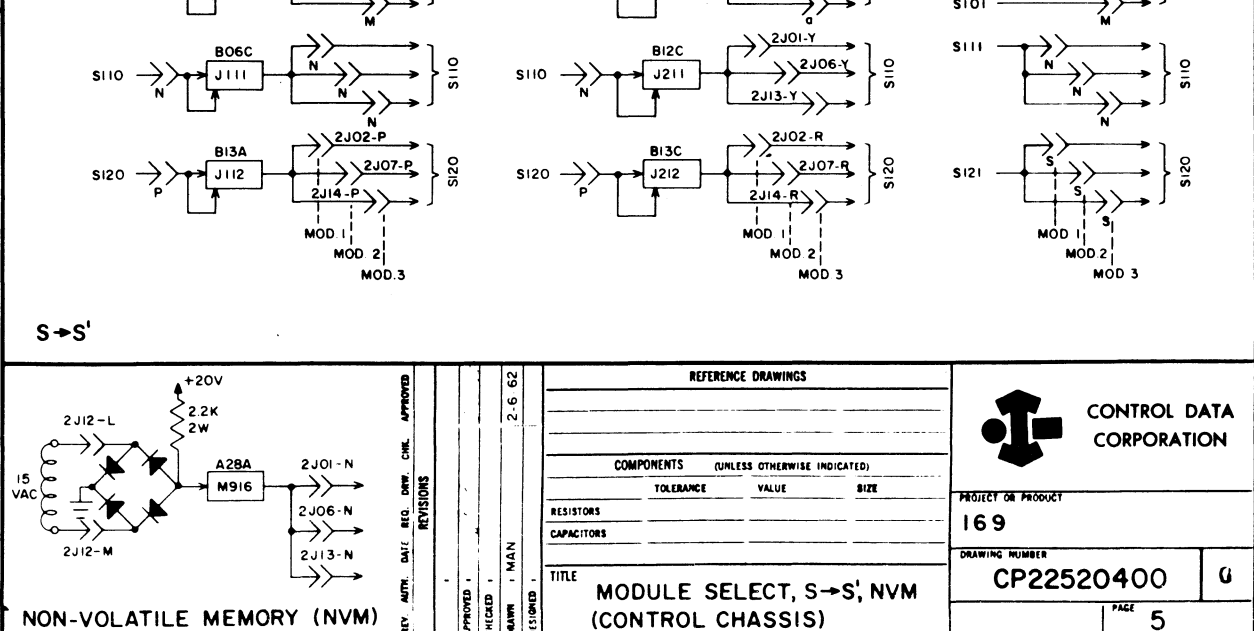
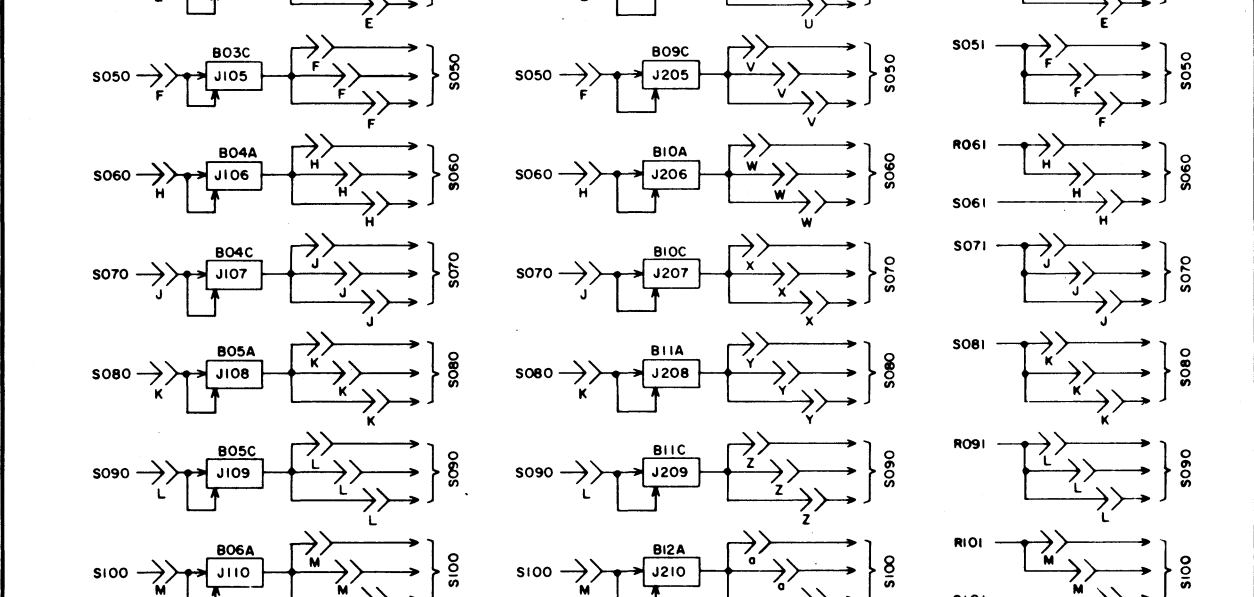
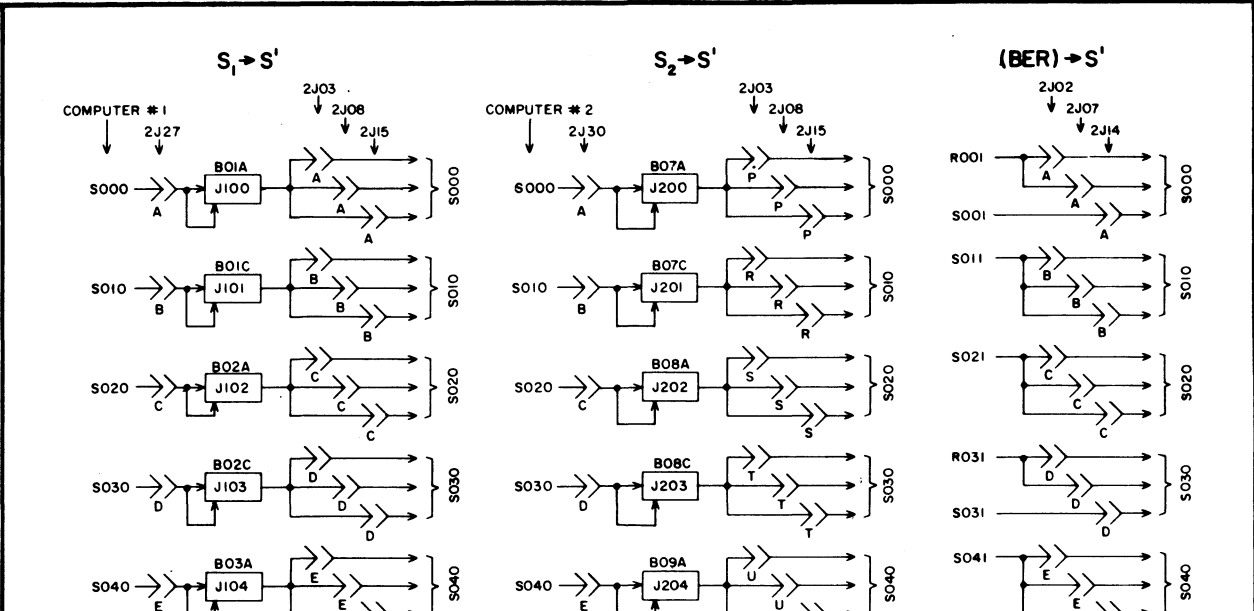


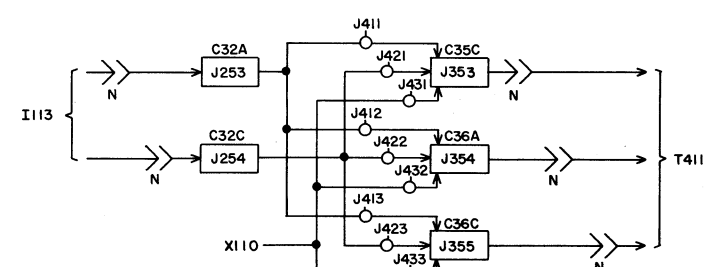
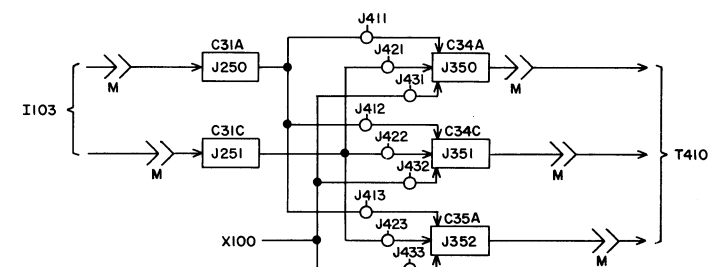
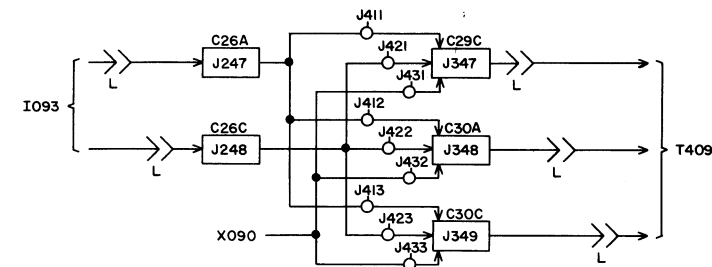
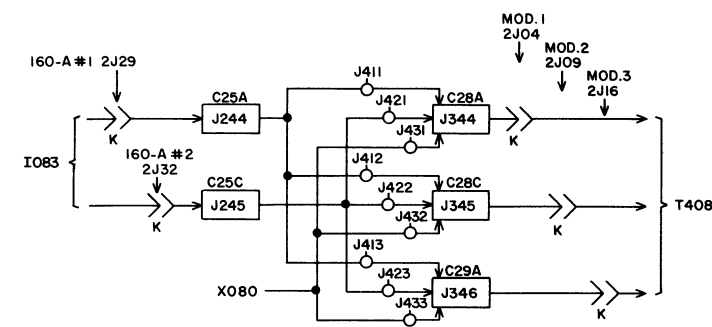
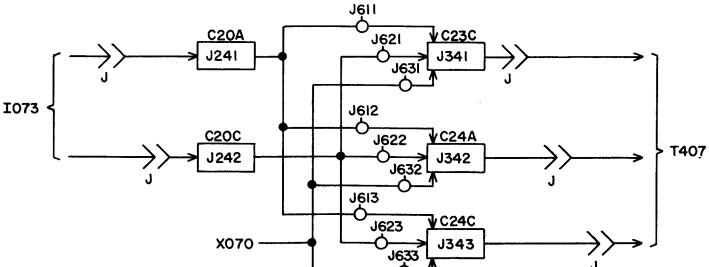
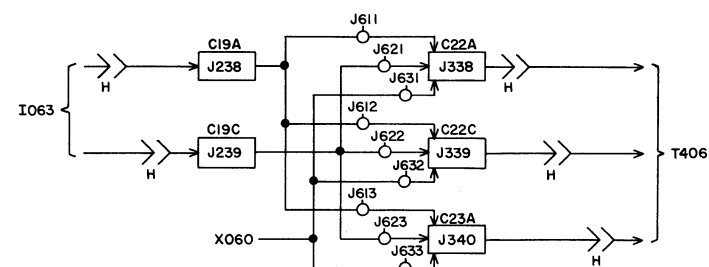
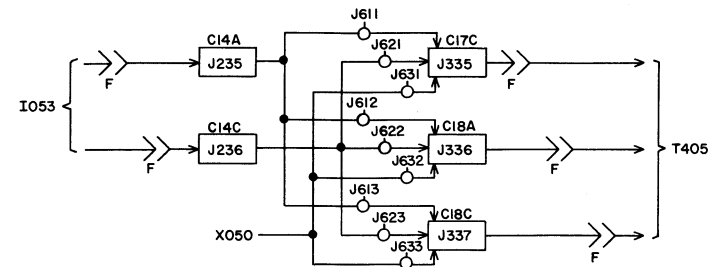
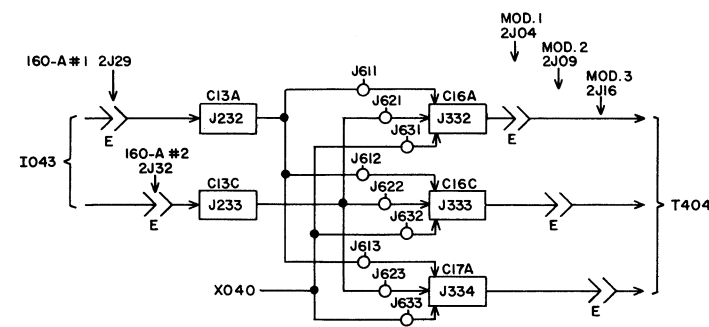
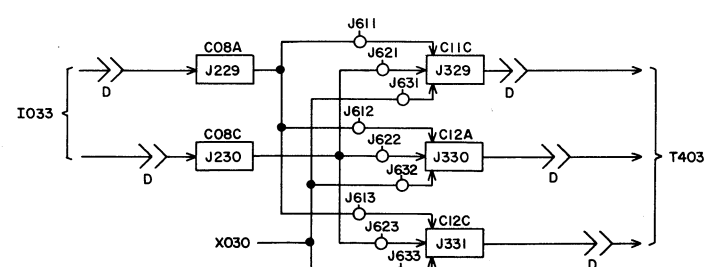
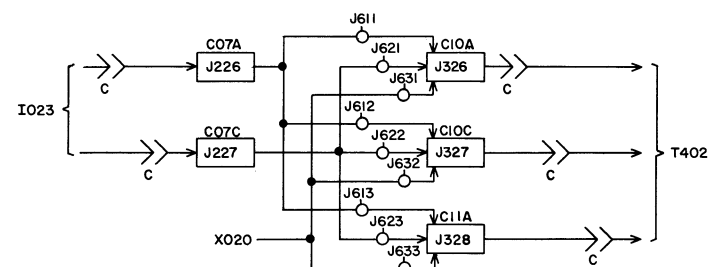
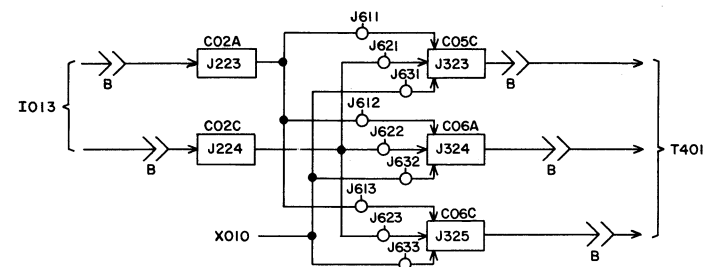
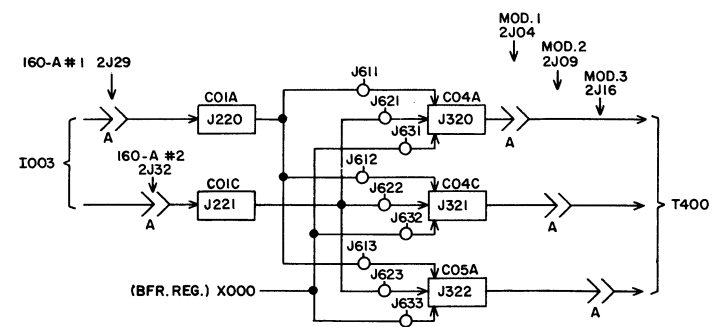
3103

YCP225202

STORAGE TRANSLATORS
(EXTERNAL MODULE CHASSIS)



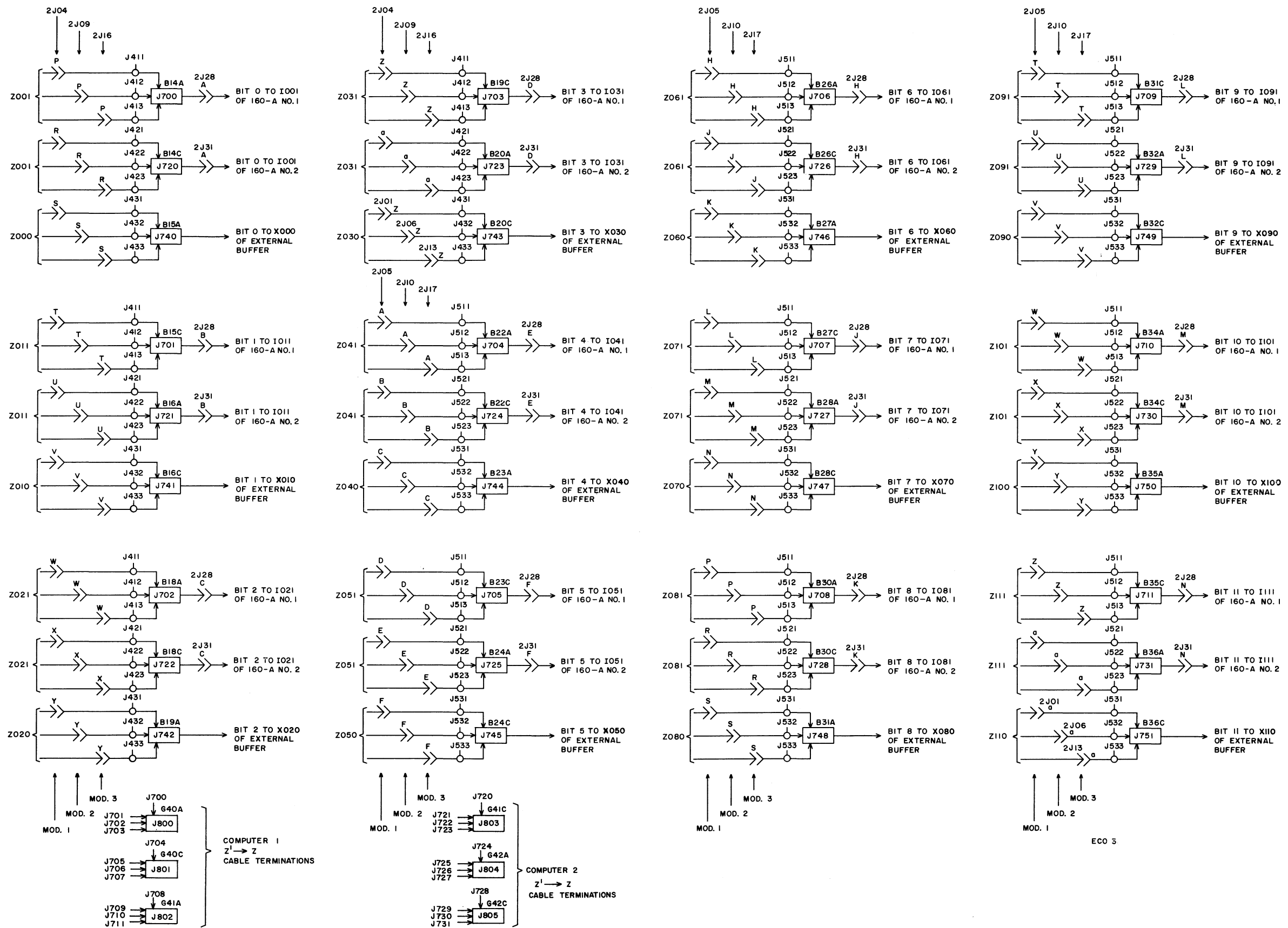




3103

YCP225205

Z → MOD'
(CONTROL CHASSIS)



3103

YCP225206

Z' → Z
(CONTROL CHASSIS)

INTERRUPT 1

INTERRUPT 2

[illegible]

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
TOLERANCE	VALUE	SIZE	
RESISTORS			
CAPACITORS			
TITLE			
BUFFER SELECT, INTERRUPT, & CONTROL WORD GATING (CONTROL CHASSIS)			

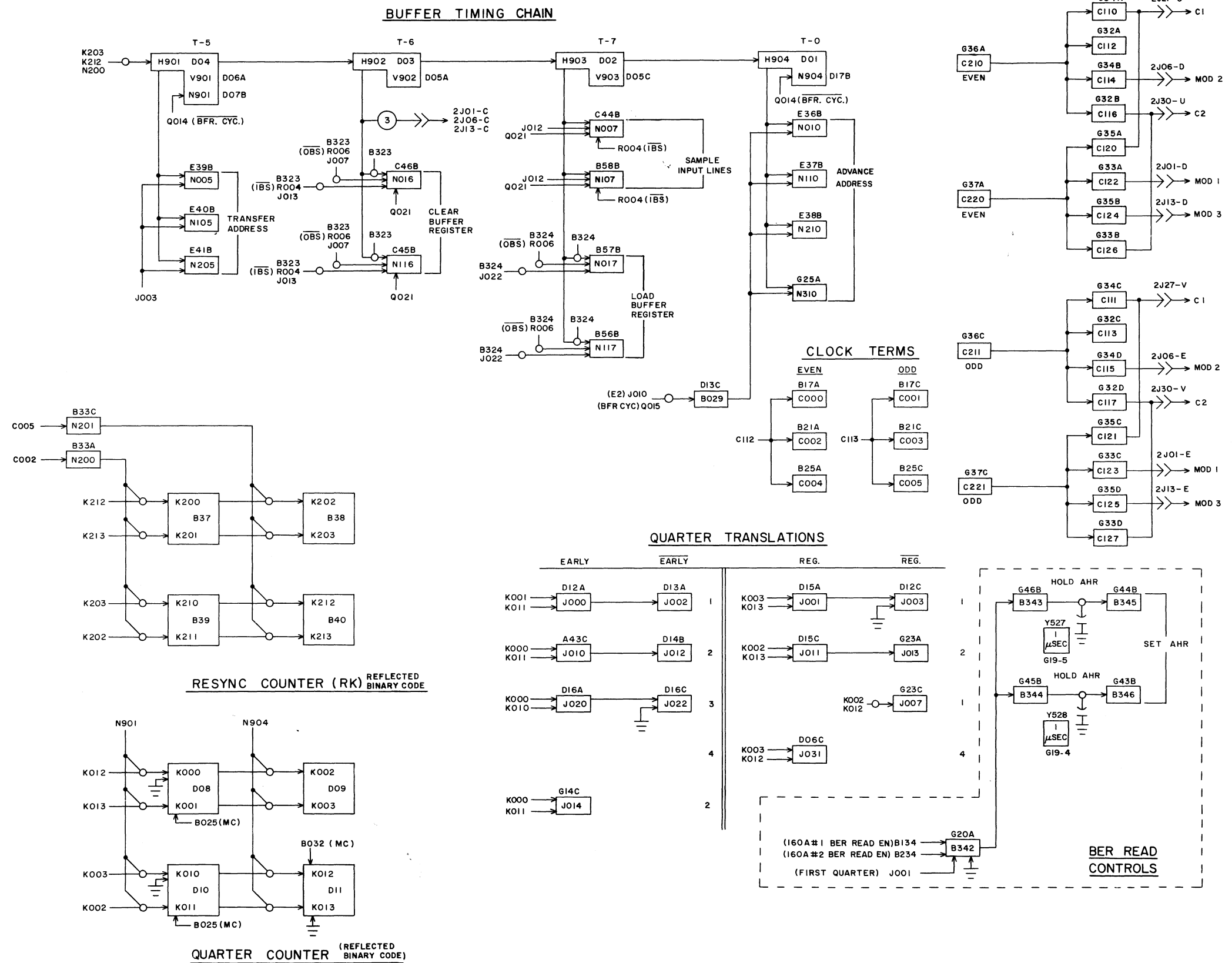


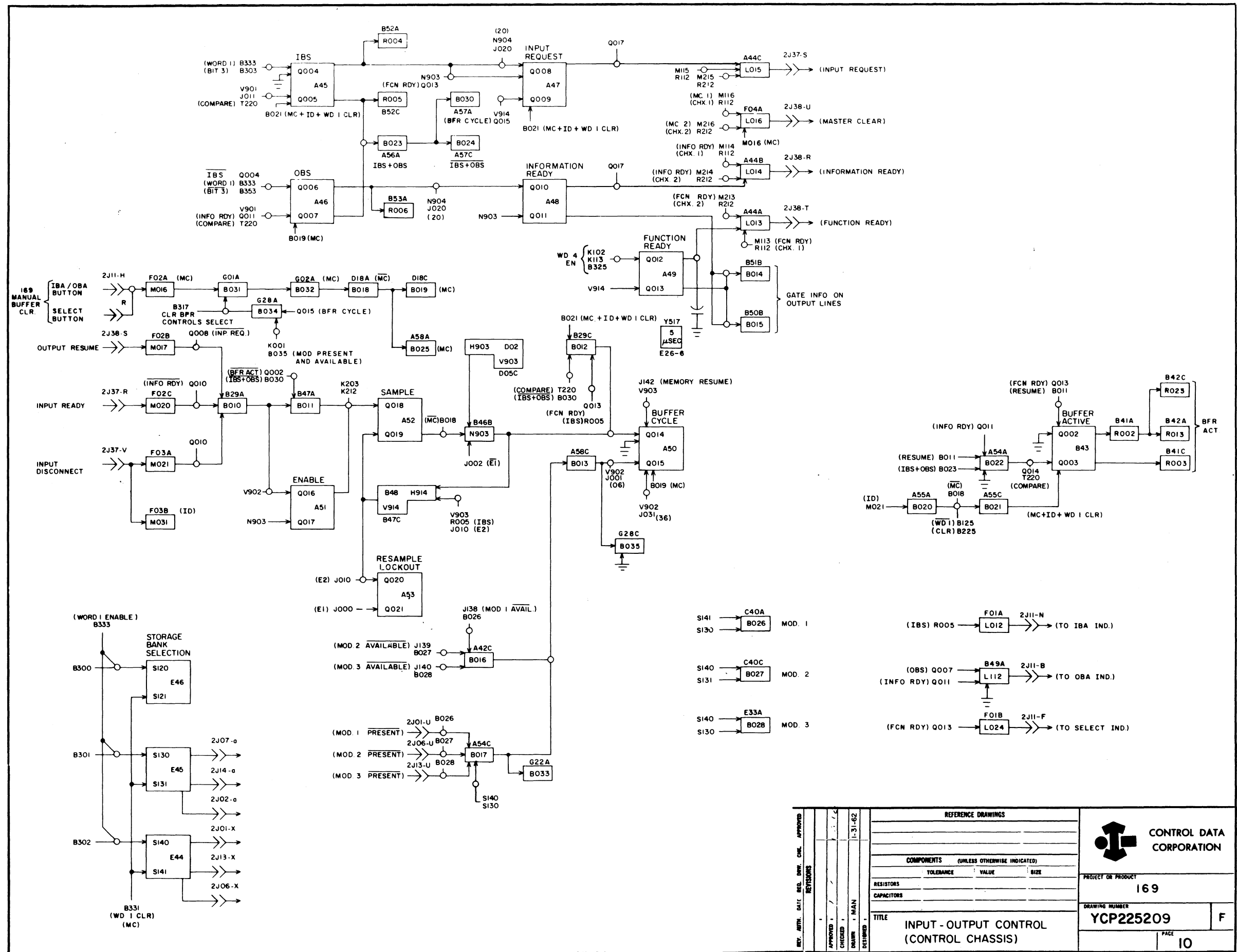
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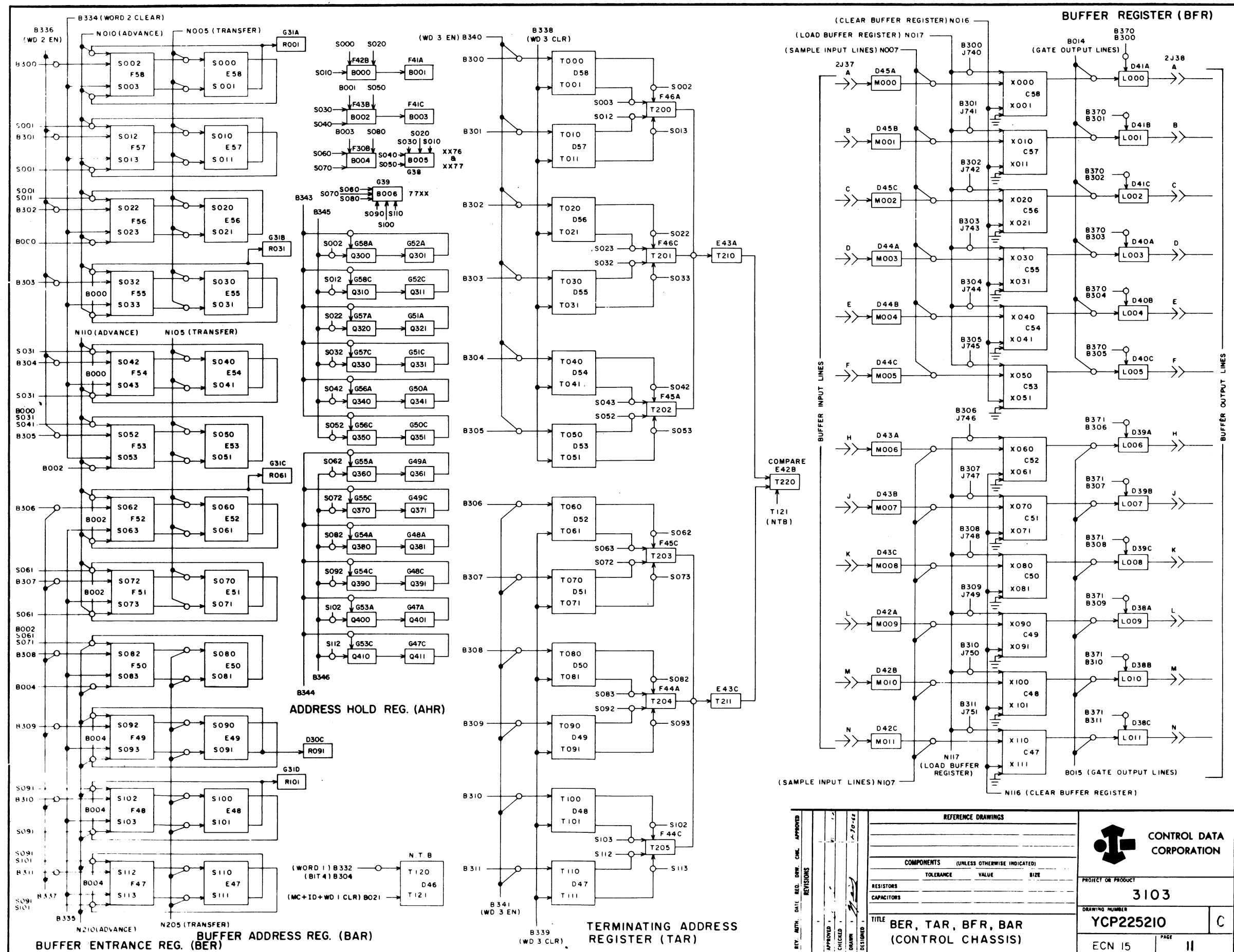
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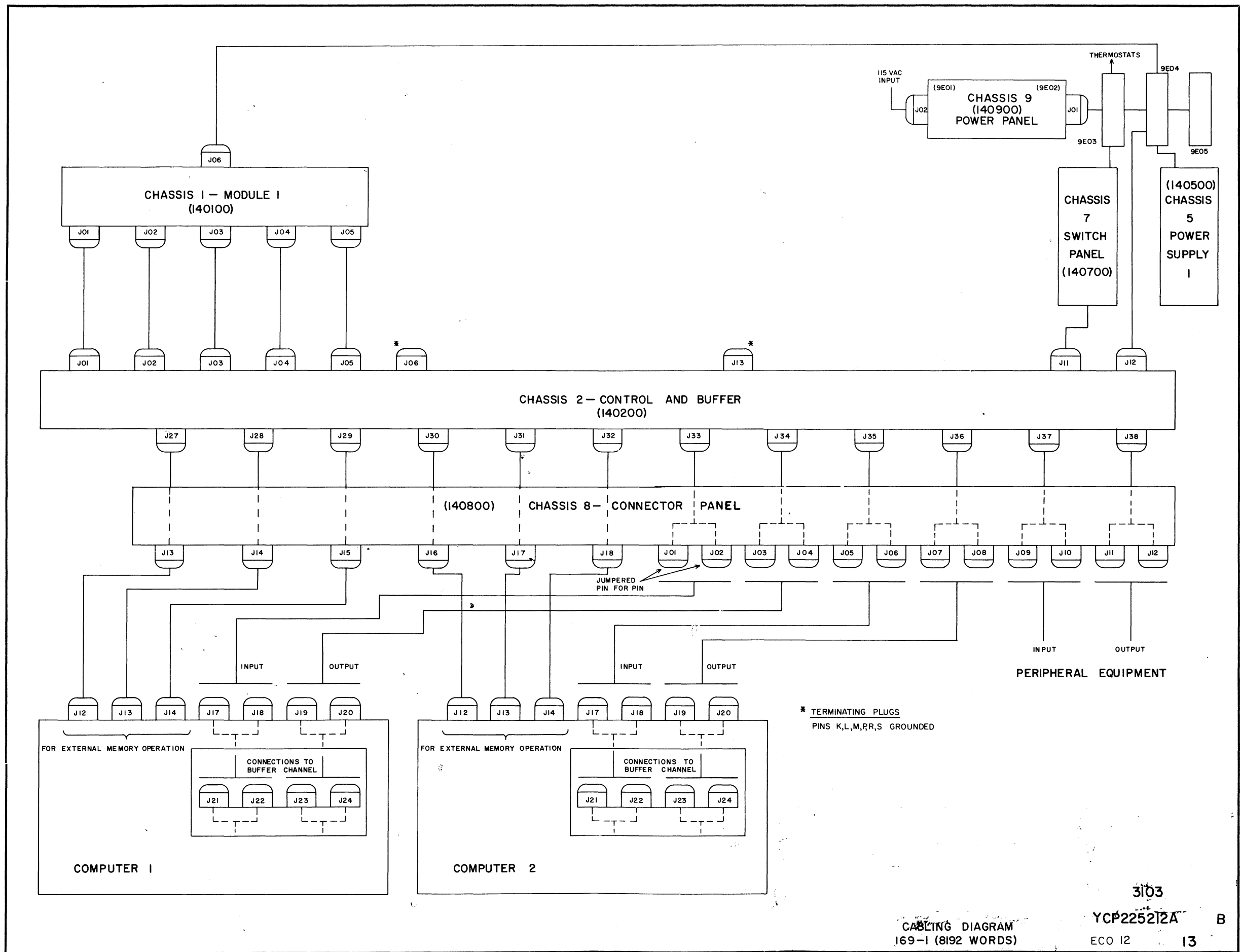
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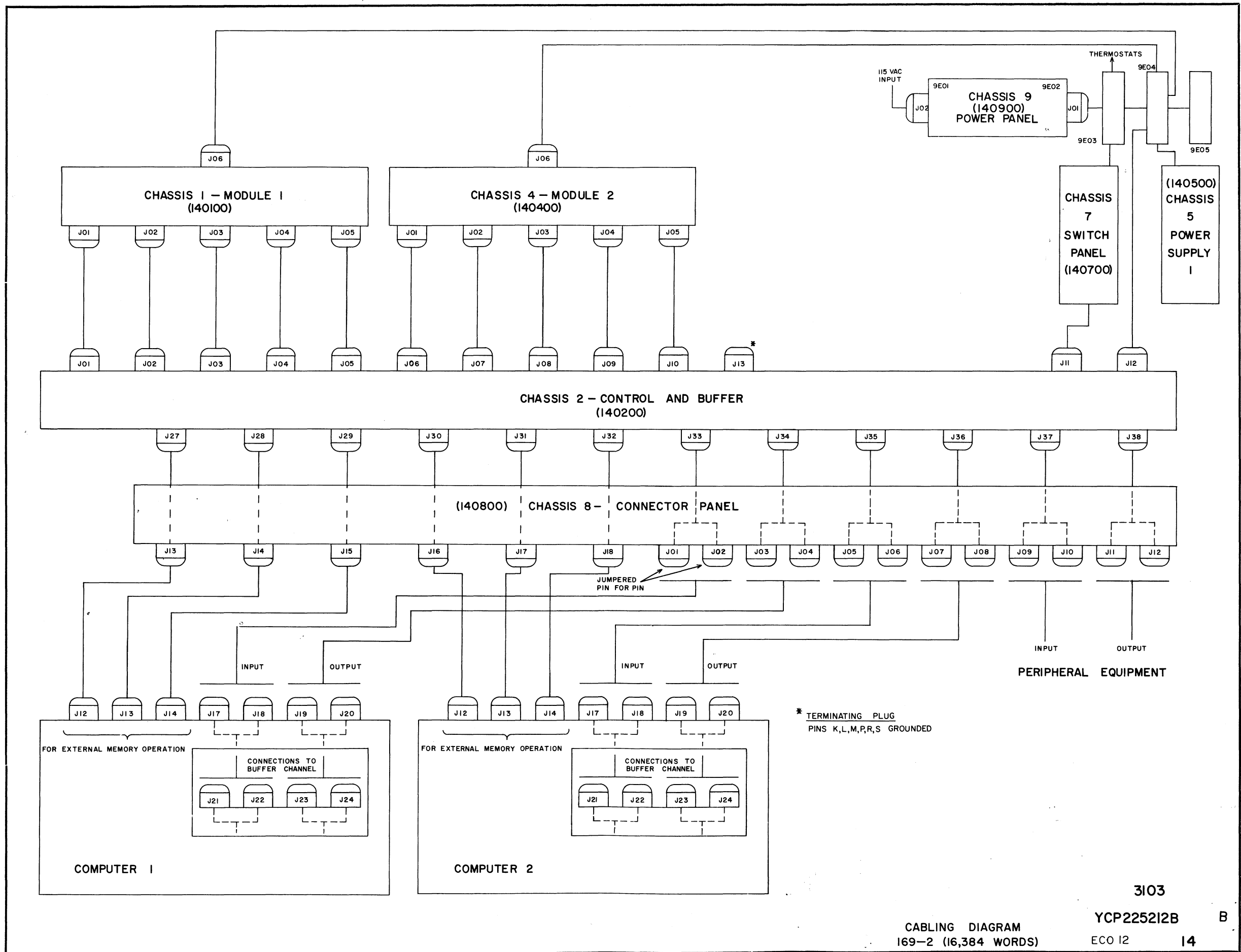
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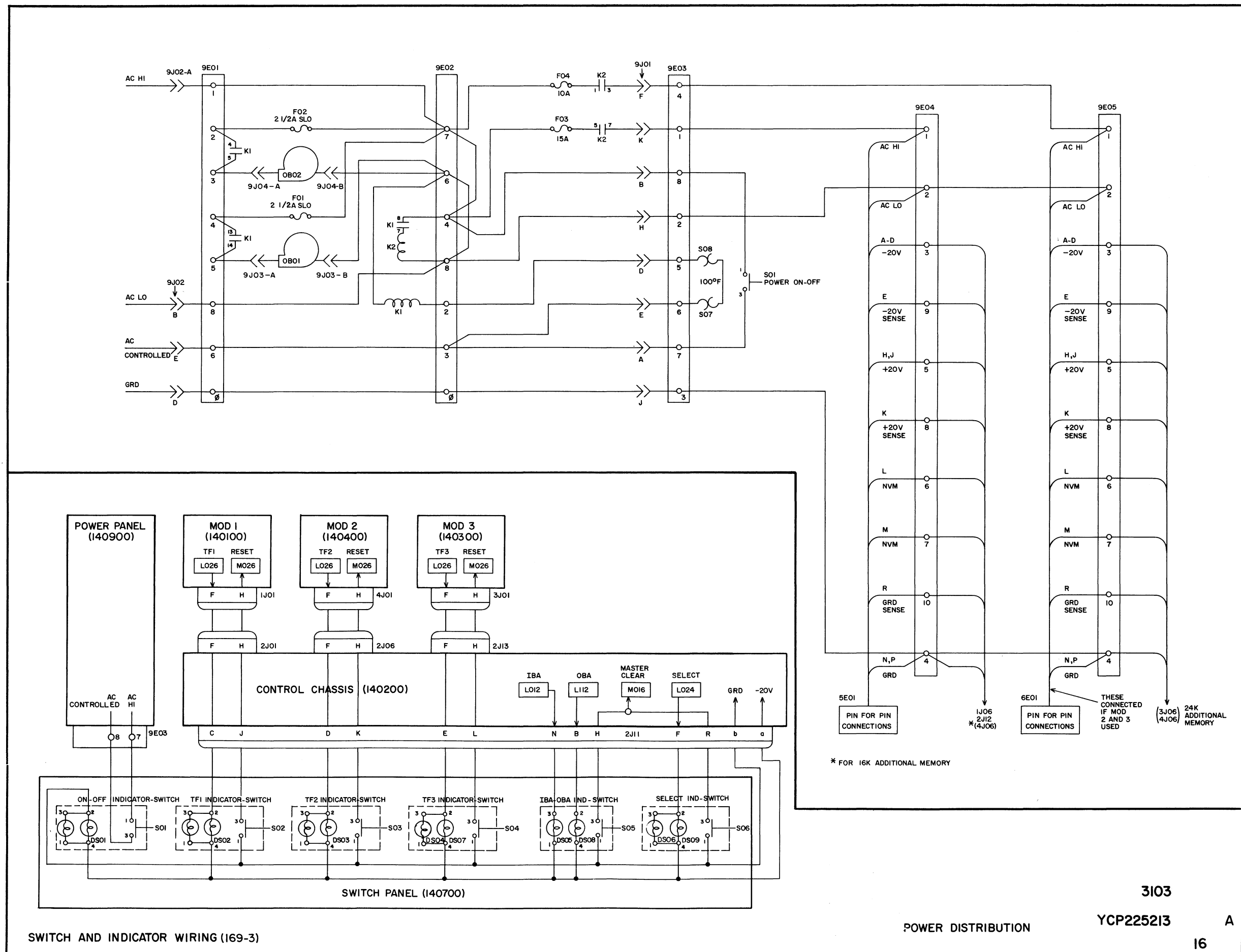












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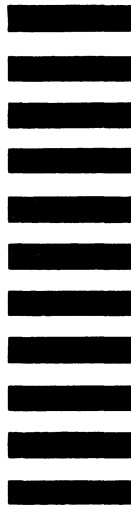
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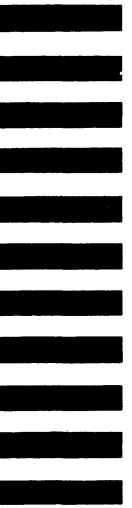
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